REMARKS

This paper is responsive to a non-final Office action dated March 11, 2004. Claims 1-20 were examined and stand rejected. Applicant has made non-narrowing amendments to claims 1, 9, and 17 to clarify the claims, and not to overcome the art of record. Applicant has also added new claims 21 – 31. Applicant has also amended the specification. No new matter has been added.

Rejections under 35 U.S.C. §102(e)

The Office has rejected claims 1 – 5, 8, 9, 11 – 14, 17, 19, 20 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,487,639 issued to Lipasti (hereinafter referred to as "Lipasti"). Applicant respectfully traverses all rejections.

The Office's rejections cannot stand because Lipasti does not disclose or suggest 1) a scoreboard despite the Office's improper interpretation of scoreboard, 2) associating an instruction with an index value as mistakenly argued in the Office action, and 3) invalidating a scoreboard entry as recited in Applicant's claims.

1) Lipasti fails to disclose or suggest a scoreboard

Lipasti discloses a value prediction table, but does not disclose a scoreboard. The Office states that it will treat the term "scoreboard" as a label for any table, including the value prediction table or cache disclosed by Lipasti. Applicant respectfully submits that the Office's characterization of Applicant's term is improper. The Office goes so far as to even suggest a completely different term for the claim. One of ordinary skill in the art would recognize the meaning of the term scoreboard. A scoreboard relates to dependencies between operations and not value prediction. The Office cannot change Applicant's claims to conform to a reference. Applicant's claim recites "scoreboard" and does not recite "value prediction table." The Office must examine Applicant's claims as they appear, and Lipasti does not disclose or suggest a scoreboard.

2) The Office fractures Applicant's claims and mistakenly argues that Lipasti discloses associating an index with an instruction

The Office fractures Applicant's claims and examines isolated terms. The Office isolates the term "associating" and states that associating "is interpreted as any information or operation being used related to the instruction." However, Applicant specifically claims "associating an instruction with an index value" as recited in claim 1, and similarly recited in claims 9 and 17. Lipasti does not disclose an index being associated with an instruction. Lipasti discloses deriving an index from an instruction, but deriving is not the same as associating. Moreover, Applicant respectfully submits that it would be extraneous to derive an index from an instruction, and then associate the index with the instruction that is the source of the index.

In addition, the Office mistakenly states that the load data address of a load instruction is an index to the load instruction. Actually, Lipasti discloses two structures: a predicted value table and a cache. The predicted value table is indexed by at least a part of program counters. The cache is indexed with load data addresses. Neither of the structures disclosed by Lipasti indicate instructions, hence the indices cannot index instructions (Figure 3, col. 6, lines 3 – 19, col. 6 lines 59 – 67). The program counters index entries that indicate a tag value, a confidence value, and a predicted value. The load data addresses index entries that indicate a tag value, a valid bit, and a data value. **None of these entries indicate a load instruction as stated by the Office action**, and Lipasti never discloses or suggests associating an index with an instruction.

3) Lipasti fails to disclose or suggest terminating the scoreboard entry associated with the instruction associated with the terminating event

Again, the Office fractures Applicant's claims into individual terms and examines isolated terms to reject the entire claim. The Office mistakenly assumes that Lipasti discloses "invalidating the scoreboard entry" as recited in claim 1, and similarly in claims 9 and 17. As already stated, Lipasti does not disclose a scoreboard. Ignoring the absence of a scoreboard in Lipasti, the Office refers to the section of Lipasti that discloses a hit or miss in cache in conjunction with availability of a predicted value to support the argument that Lipasti discloses a terminating event, even though a cache miss is not a terminating event. The return of the data from memory after a cache miss is an example of a terminating event. Applicant's claims recite

receiving an indication of a "terminating event associated with the instruction and invalidating the scoreboard entry." Lipasti does not invalidate any entries in its value prediction table. Lipasti discloses determining if an entry is valid, but does not disclose invalidating an entry. Furthermore, Applicant's claim recites receiving an indication of a terminating event associated with an instruction and invalidating the scoreboard entry, which has been associated with the instruction. Lipasti does not disclose or suggest "invalidating the scoreboard entry associated with the instruction associated with the terminating event" as recited in claim 1, and similarly in claims 9 and 17.

Lipasti does not anticipate Applicant's claims. For at least the reasons above, Applicant's independent claims are allowable over the art of record. In addition, all of the dependent claims are at least allowable because they depend from corresponding ones of the above allowable independent claims.

Rejections under 35 U.S.C. §103(a)

The Office has rejected claims 6, 7, 15, 16, and 18 under 35 U.S.C. §103(a) as being unpatentable over Lipasti in view of U.S. Patent No. 6,473,832 issued to Ramagopal et al (hereinafter referred to as "Ramagopal"). Applicant respectfully traverses all rejections.

The Office attempts to supports its rejection of claims 6, 7, 15, 16 and 18 by simply adding Ramagopal's disclosure of a load store unit. Neither Lipasti nor Ramagopal disclose or suggest "forwarding the instruction and the index value to a load/store processing unit" as recited in claims 6, 15 and similarly in claim 18 or "receiving the index value from a load/store processing unit" as recited in claims 7, 16 and similarly in claim 18. One of the basic criteria for an obviousness rejection is that the prior art reference must teach or suggest all of the claim limitations (MPEP 2143). "Although a prior art device 'may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so'" (MPEP 2143.01, *quoting* In re Mills, 916 F.2d 680 (Fed. Cir. 1990)). Since Lipasti and Ramagopal lack such suggestions or motivation to achieve Applicant's claimed invention, the Office assumes, without any evidentiary support in the record, that it would have been obvious to one of ordinary skill in the art to modify Lipasti and Ramagopal to achieve Applicant's invention. Indeed, "[i]t is never appropriate to rely solely on 'common knowledge' in the art

without evidentiary support in the record, as the principal evidence upon which a rejection was based" (MPEP 2144.03, *citing* In re Zurko, 258 F.3d 1379 (Fed. Cir. 2001). "[A]n assessment of basic knowledge and common sense that is not based on any evidence in the record lacks substantial evidence support" (MPEP 2144.03, citing Id.).

The Office assumes that since Lipasti discloses forwarding a load data address to a comparator, then it would be obvious to forward the load data address to a load store unit of Ramagopal. It would be redundant to forward a load data address to a load store unit because the corresponding load instruction, which indicates the load data address, is already sent to the load store unit. Therefore, there is no support for the argument that the combination of Lipasti and Ramogopal teaches or suggests forwarding a load data address and an instruction to a load store unit. Similarly, there is no explanation for returning an index from a load store unit to either the data table or the predicted value table in Lipasti. The predicted table has already been accessed to acquire a predicted value, so returning an index from a load store unit to the predicted table conflicts with the principle of operation of the predicted table. In addition, the cache has already been accessed coincident with access to the predicted value table. The results of accessing the cache drive the predicted value. It would fail reason to send a load address to a cache, and then have a load store unit return another load address to the cache.

Conclusion

In summary, claims 1-31 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Respectfully submitted,

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